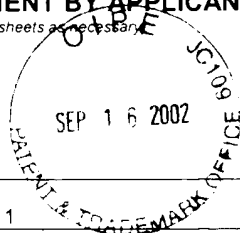


Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)



Complete if Known

Application Number	09/893023
Filing Date	June 27, 2001
First Named Inventor	O'Mahony, Frank
Group Art Unit	2812
Examiner Name	Unknown

Sheet 1 of 1

Attorney Docket No: 00884.405US1

**US PATENT DOCUMENTS**

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
A.S.	US-5387885	02/07/1995	Chi, V.L.	333	100	05/25/1993
	US-5410491	04/25/1995	Minami, F.	364	491	06/10/1992
	US-5519351	05/21/1996	Matsumoto, H.	327	295	11/10/1994
	US-5521541	05/28/1996	Okamura, H.	327	297	02/15/1994
	US-5570045	10/29/1996	Erdal, A.C., et al	326	93	06/07/1995
	US-5668484	09/16/1997	Nomura, M.	326	93	09/16/1994
	US-5691662	11/25/1997	Soboleski, A.J., et al	327	292	04/15/1996
	US-5717229	02/10/1998	Zhu, Q.	257	208	03/26/1996
	US-6043704	03/28/2000	Yoshitake, A.	327	565	07/07/1998
	US-6150865	11/21/2000	Fluxman, S., et al	327	292	07/09/1999
	US-6157688	12/05/2000	Tamura, H., et al	375	348	10/06/1997
	US-6311313	10/30/2001	Camporese et al	716	6	12/29/1998
	US-6323714	11/27/2001	Naffziger, S.D., et al	327	295	02/03/2000

**FOREIGN PATENT DOCUMENTS**

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T <sup>2</sup>
--------------------	---------------------	------------------	---	-------	----------	----------------

**OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
A.S.		BAKOGLU, H.B., <u>Circuits, Interconnections, and Packaging for VLSI</u> , Addison-Wesley Publishing Company, (1990), Table of Contents	
AS.		BERNSTEIN, K., et al., <u>High Speed CMOS Design Styles</u> , Kluwer Academic Publishers, (1998), Table of Contents	

EXAMINER

AS

DATE CONSIDERED

12.23.02

Substitute Disclosure Statement Form (PTO-1449)

\* EXAMINER: Initial if reference considered whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. \* Applicant's unique citation designation number (optional): 2. Applicant is to place a check mark here if English language Translation is attached.